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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): MCT.0047C1US (99.0404.01US)

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on January 23, 2006

Signature: Janice Munoz

Typed or printed name: Janice Munoz

Application Number	Filed
10/651,324	August 28, 2003

First Named Inventor: Christopher K. Morzano

Art Unit	Examiner
2188	Mardochee Chery

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 40,779
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34

Signature

Fred G. Pruner, Jr.
Typed or printed name

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Telephone number

January 23, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [x] *Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Christopher K. Morzano	§	Group Art Unit:	2188
		§		
Serial No.:	10/651,324	§		
		§	Examiner:	Mardochee Chery
Filed:	August 28, 2003	§		
		§		
For:	System And Method To Reduce Cycle Time By Performing Column Redundancy Checks During A Delay To Accommodate Variations In Timing Of Data Strobe Signal	§	Atty. Dkt. No.:	MCT.0047C1US (99.0404.01/US)

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REASONS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Applicant seeks pre-appeal review of the rejections of claims 37-71. Claims 1 and 37-71 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Roy in view of Hsu. The § 103(a) rejections of claims 37-71 are addressed below.

§ 103 Rejections of Claims 37-42:

In order to establish a *prima facie* case of obviousness, the prior art must teach or suggest all claim limitations. M.P.E.P. § 2143.03.

Neither Roy nor Hsu teaches or suggests the combination of performing a column redundancy check and synchronizing the beginning of an internal write operation to a memory cell array of a memory device to a clock signal. In the Final Office Action, the Examiner contends that Roy allegedly clearly discloses synchronizing a data transfer to a clock signal.

Date of Deposit: January 21, 2006
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Janice Munoz

Janice Munoz

While this may be generally true, Roy fails to teach or suggest synchronizing the beginning of an internal write operation to a memory cell array of a memory device to a clock signal.

Roy generally describes a multichannel memory architecture that includes a boundary 1 that defines an interface between a memory device 20 and one or more master devices 10 and 15. *See, for example*, Fig. 1 of Roy and the corresponding text in lines 40-47 in column 9 of Roy. Therefore, the language cited by the Examiner, i.e., the language found in lines 26-29 and 10-12 in column 12, relates to clock synchronization for data transfer across a boundary between memory devices, not the synchronization of the beginning of an internal write operation to a memory cell of a memory device.

Thus, Roy is directed to synchronizing a data transfer across a boundary, and the language of Roy cited by the Examiner has no relevance regarding the *synchronization of an internal write operation to a memory cell array of a memory device* to a clock signal (*emphasis added*).

Hsu fails to teach or suggest the missing claim limitations. Hsu discloses a normal bit-line selector signal (called "YS") and a redundancy bit-line selector signal (called "YSR") that enable a read/write operation. Hsu, 3:14-17. However, as depicted in Fig. 6 of Hsu, the enablement of the read/write operation does not occur in connection with the beginning of an internal write operation.

Therefore, for at least the reason that the combination of Roy and Hsu fails to teach or suggest all claim limitations; a *prima facie* case of obviousness has not been established for independent claim 37. Claims 38-42 are patentable for at least the reason that these claims depend from an allowable claim.

§ 103 Rejections of Claims 43-51:

The method of independent claim 43 recites performing a column redundancy check prior to the initiation of the providing of column select signals that are indicative of a column address to a memory cell array of a memory device.

In the Final Office Action, the Examiner refers to Roy for the general teaching of providing column select signals and relies on Hsu to allegedly teach or suggest performing a column redundancy check prior to the initiation of the providing of the column select signals. In essence, the Examiner is contending that Hsu somehow implies that the column redundancy check is initiated prior to the providing of column select signals. However, the Examiner provides no support for this reasoning. Therefore, a *prima facie* case of obviousness has not

been established for independent claim 43, as the hypothetical combination of Roy and Hsu fails to teach or suggest all claim limitations.

Claims 44-51 are patentable for at least the reason that these claims depend from an allowance claim. Therefore, for at least the reasons that are set forth above, withdrawal of the § 103(a) rejections of claims 43-51 is requested.

§ 103 Rejections of Claims 52-57:

For at least the same reasons that are set forth above for independent claim 37, the hypothetical combination of Roy and Hsu fails to teach or suggest all claim limitations. Therefore, for at least this reason, a *prima facie* case of obviousness has not been set forth for independent claim 52. In particular, the hypothetical combination of Roy and Hsu fails to teach or suggest a circuit to synchronize an initiation of an internal write operation to a memory cell array of a memory device with a clock signal. Therefore, for at least this reason, a *prima facie* case of obviousness has not been established for independent claim 53.

Claims 54-57 are patentable for at least the reason that these claims depend from an allowable claim.

§ 103 Rejections of Claims 58-64:

A *prima facie* case of obviousness has not been established for independent claim 58 for at least the reason that the Examiner fails to show where the prior art teaches or suggests a control circuit that performs a column redundancy check during a delay to accommodate variations in the timing of a data strobe signal. In this regard, the Examiner fails to establish why one skilled in the art would have modified Roy in view of Hsu so that Roy's memory system performs a column redundancy check while one or more of its CLKIN pulses are occurring. On page 3 of the Final Office Action, the Examiner states that the general motivation to combine Roy and Hsu is provided by both references allegedly being related to timing and clock operations in a memory device. However, even assuming a suggestion or motivation exists for the general hypothetical combination of Roy and Hsu, this combination does not specifically teach all the limitations (such as the control circuit) of independent claim 58. Therefore, a *prima facie* case of obviousness has not been established for claim 58.

Claims 59-64 are patentable for at least the reason that these claims depend from an allowable claim.

§ 103 Rejections of Claims 65-71:

The computer system of independent claim 65 includes a memory device that is coupled to a memory bus and is adapted to establish a predetermined window of time to capture data and perform a column redundancy check in response to the memory operation during the predetermined window of time.

A *prima facie* case of obviousness has not been established for independent claim 65 for at least the reason that the prior art fails to teach or suggest the memory device of claim 65. In particular, to purportedly show where the prior art teaches the predetermined window of time of claim 65, the Examiner refers to the alleged necessity in Roy to hold bytes "within the input data buffer unit 178 for a period of time before sending the data for synchronization of the I/O write operation with the column select signal 181." Final Office Action, 13. However, the Examiner fails to show why one skilled in the art would have performed a column redundancy check during this alleged holding time. Hsu fails to teach or suggest the missing claim limitations. Therefore, a *prima facie* case of obviousness has not been established for independent claim 65.

Claims 66-71 are patentable for at least the reason that these claims depend from an allowable claim

Respectfully submitted,

Date: January 23, 2006

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